REMARKS

Applicants would like to thank Examiner for the courtesy of a telephone interview today, during which Examiner indicated that a new search would be performed pursuant to the amendments to claim 1, and Applicants notified of the results, by the 6-month deadline of the current Office Action.

The Abstract has been amended as requested, to delete the words "system includes." No new matter has been added.

Applicants thank Examiner for allowing claims 2-10.

Claim 1 is rejected under 25 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,275,415 to *Haddad et al.* ("*Haddad*"). Applicants respectfully traverse, noting that *Haddad* does not disclose every element of claim 1 as amended. More specifically, *Haddad* does not disclose applying an incremental current to bitlines of selected memory cells, where the incremental current is substantially equal to leakage current from those same bitlines.

Haddad discloses a programmable memory cell circuit (*e.g.*, FIG. 6). Memory cells or transistors 602, 604, 606, 608 are connected to a bitline BL. When a particular transistor, say 604, is to be programmed, a programming current I_2 is passed through the transistor 604 and onto the bitline BL. At the same time, small leakage currents I_1, I_3, I_4 flow through the transistors and onto the bitline BL, so that $I_{BL} = I_1 + I_2 + I_3 + I_4$.

Note that, in the system of *Haddad*, the leakage currents never pass through the cell being programmed. Instead, they only pass through other cells. That is, during the programming of cell 604, the only current passing through that cell is the programming current I_2. The leakage currents I_1, I_3, I_4 pass through the remaining cells 602, 606, 608, and not cell 604.

In contrast, claim 1 recites "applying an incremental current to selected memory cells during programming of said selected memory cells," (emphasis added) where the incremental current is "substantially equal to leakage current from said selected memory cells." Accordingly, *Haddad* does not disclose every element of claim 1 as amended.

CONCLUSION

In view of the above, it is respectfully submitted that Claims 1-10 are now in condition for allowance.

The Examiner is invited to call Applicant's attorney at the number below in order to speed the prosecution of this application.

The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to Deposit Account **No. 07-1896** referencing, **351913-992980** (Formerly 2102397-992980).

Respectfully submitted,

DLA PIPER RUDNICK GRAY CARY US LLP

Dated: January 24, 2006 By _____
Jon Y. Ikegami
Reg. No. 51,115
Attorney for Applicants

DLA PIPER RUDNICK GRAY CARY US LLP
2000 University Avenue
East Palo Alto, CA 94303
650-833-2104 (Direct)
650-833-2000 (Main)
650-833-2001 (Facsimile)
jon.ikegami@dlapiper.com